

**Title:**        **TEST REGION LAYOUT FOR SHALLOW TRENCH ISOLATION**

**FIELD OF INVENTION**

[0001]        The present invention relates to test areas of wafers used during semiconductor manufacturing.

**BACKGROUND OF THE INVENTION**

[0002]        Referring generally to Fig. 1, shallow trench isolation (STI) is an enabling technology for the fabrication of advanced sub-micron integrated devices. A typical STI process sequence includes the following process steps: pad oxide oxidation, LPCVD nitride deposition, trench lithography, trench etch, resist strip/clean, liner oxidation, CVD oxide trench fill, planarization, post-chemical mechanical polishing (CMP) clean/light BHF dip, and nitride strip. This sequence describes STI related processes only and leaves out many other front-end processing steps.

[0003]        Requirements for STI planarization are much more stringent than those for inter-layer dielectric (ILD) planarization. CMP has been accepted in recent years as a critical step in mainstream integrated circuit fabrication technology, and has enabled the fabrication of multi-level interconnection of up to 5 or 6 metal levels.

[0004]        Superior isolation characteristics of STI enable scaling of active area pitches to the 0.5 mm regime. This, coupled with the additional advantages of better planarity, latch-up immunity, low junction capacitance, and a near-zero-field encroachment mandates the use of STI in advanced complementary metal-oxide semiconductor (CMOS) technologies.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0005] Fig. 1 is a side planar view in cutaway of a typical STI fabrication sequence;

[0006] Fig. 2 is a top view of an exemplary set of test regions and a test area; and

[0007] Fig. 3 is a top view of an exemplary set of test regions and a test area.

### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0008] Referring now to Fig. 2, in an embodiment a gap fill test pattern such as for a shallow trench isolation (STI) gap fill comprises one or more test regions 10,20. Each test region 10,20 further comprises an outer circumference (e.g. comprising sides 11 and 12 or sides 21 and 22) defining first interior area 19,29 and test pattern 18,28 disposed in first interior area 19,29.

[0009] Test region 10,20 may comprise a square rectangular region 10, a non-square rectangular region 20, a substantially orthogonal region 20, or the like, or a combination thereof.

[0010] In certain embodiments, square rectangular region 10 comprises an area of around  $1\ \mu\text{m}^2$  and test pattern border 17 defines a square comprising an area of around  $0.09\ \mu\text{m}^2$ , i.e. sides 11 and 12 are around  $0.3\ \mu\text{m}$ . Width 13 may range from around  $0.085\ \mu\text{m}$  to around  $0.200\ \mu\text{m}$ .

[0011] In other embodiments, a non-square rectangular region 20 may comprise an area of around from around  $1\ \mu\text{m}^2$  to around  $3\ \mu\text{m}^2$  and test pattern 28 may define a rectangle, comprising border 27 comprising width 23 ranging from around  $0.085\ \mu\text{m}$  to around  $0.200\ \mu\text{m}$ . Test pattern rectangle 28 further comprises height 25 which be around one-half height 21 of non-square rectangular region 20.

[0012] Referring now to Fig. 3, border 17,27 may be a contiguous border 17 or comprise at least one discontinuity, e.g. 34,44 in border 17,27.

[0013] Test regions 10,20 which comprise a contiguous border 17,27 (Fig. 2) may be adapted to simulate a corner region of a static random access memory cell (not shown in the figures). Test regions 10,20 which comprise at least one discontinuity 34,44 may be adapted to simulate an outer diameter line end region of a static random access memory cell (not shown in the figures). Discontinuity 34,44 may be configured as a gap of around 0.1  $\mu\text{m}$ .

[0014] In certain embodiments, a plurality of discontinuities 34,44 may be present in test pattern 18,28, defining a plurality of discontinuous border segments 37,38 and 47,48. Each border segment 37,38 and 47,48 may further comprise a first section intersecting a second section. In a preferred embodiment the first section intersects the second section at a substantially right angle.

[0015] Each test pattern 18,28 may be fabricated using a shallow trench adapted for testing of shallow trench isolation gap fill, the test pattern (18,28) defining a border (17,27) to a second interior area (16,26).

[0016] Referring to either Fig. 2 or Fig. 3, a gap fill test region pattern for an STI gap fill may comprise test area 100 fabricated on a predetermined region of a semiconductor wafer. Test area 100 may further comprise border 101 and first interior area 102. A plurality of test regions 10,20 may be disposed within first interior area 102, the test regions 10,20 comprising second interior area 19,29 and border 17,27 where border 17,27 defines third interior area 16,236, the test pattern further comprising at least one shallow trench adapted for testing of shallow trench isolation gap fill.

[0017] Test area 100 may further comprise and/or define a grid comprising one or more grids, e.g. 112,114,116, the grids further defining a predetermined number of columns and rows within the fabricated test area 100.

[0018] An array of first rectangular test regions 10,20 may be disposed within a grid, e.g. 112, where each first rectangular test region 10,20 occupies a unique grid cell defined by a column and row of the grid. An array of second rectangular test regions 10,20 may be further disposed within the grid, e.g. 114, each second rectangular test region occupying a unique grid cell defined by a column and row of that grid 114 where the second rectangular test regions 10,20 further comprise at least one dimension which differs from the dimensions of the first rectangular test regions. For example, the first rectangular test regions 10,20 in grid 112 may be squares and the second rectangular test regions 10,20 in grid 114 may be non-square rectangles.

[0019] An array of third rectangular test regions 10,20 may be disposed within test area 100, e.g. in grid 116, where each third rectangular test region 10,20 occupies a unique grid cell defined by a column and row of grid 116. These third rectangular test regions 10,20 may further comprise at least one dimension which differs from a dimension of the first rectangular test regions 10,20, e.g. in grid 112, and at least one dimension which differs from a dimension of the second rectangular test regions 10,20, e.g. in grid 114.

[0020] It will be understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated above in order to explain the nature of this invention may be made by those skilled in the art without departing from the principle and scope of the invention as recited in the appended claims.